**Reference Papers:**

1. **Alam, M.; Kang, K.; Paul, B.C.; Roy, K.; , "Reliability- and Process-Variation Aware Design of VLSI Circuits," Physical and Failure Analysis of Integrated Circuits, 2007. IPFA 2007.**

Because of fabrication limitations, no two transistors can be exactly identical on the atomic scale. Integrated circuits vary significantly from die to die and from wafer to wafer due to process variability. In this paper, variation related issues have been broadly classified into two classes.

Time zero variation: models of process and operation – Random dopant effects, parameter variation, randomness of poly-silicon characteristics, and the randomness of drain current in nano-sized transistors are posing significant challenges to continued device scaling. To design a functional IC made of transistors with random parameters, the randomness must first be characterized. In addition to process variation, the local operating condition (e.g. inhomogeneous temperature distribution or site specific voltage loss due R-C drop in interconnects) can bring in an additional degree of randomness among the individual transistors.

Time zero variation: models of reliability – Permanent time dependent changes in the operating transistor characteristics are also important reliability issues that should be taken into account when designing a circuit. These reliability issues include radiation induced permanent damage in SRAM, generation of bulk defects leading to dielectric breakdown, and soft error issues to the NBTI stress related failures.

1. **Kumar, R.; Kursun, V.; , "Impact of temperature fluctuations on circuit characteristics in 180nm and 65nm CMOS technologies," Circuits and Systems, 2006. ISCAS 2006.**

Temperature fluctuations cause changes in the threshold voltage, carrier mobility and saturation velocity of a MOSFET. These shifts all directly affect the drain current of the devices.   
This paper identifies the device parameters that characterize the variations in MOSFET current due to temperature fluctuations in 180nm and 65nm technologies. They propose a circuit design methodology based on optimizing performance by choosing a supply voltage that is insensitive to temperature variation. The results state that the supply voltage that is ideal from a temperature fluctuation standpoint is 68%-69% lower than the nominal supply voltage in 65nm technology.

1. **Jae-Joon Kim; Rao, R.; Mukhopadhyay, S.; Ching-Te Chuang; , "Ring oscillator circuit structures for measurement of isolated NBTI/PBTI effects," Integrated Circuit Design and Technology and Tutorial, 2008.**

Degradation of device threshold voltage under electrical and thermal stress is becoming a major reliability issue. In 45nm technology, both Positive and Negative Bias Temperature Instability (PBTI and NBTI) have become of equal importance. To properly understand the impact of these two mechanisms, designers need to test them separately. This paper proposes novel circuit structures that monitor the two effects separately while conserving the simplicity of the classic ring oscillator structure. The circuit describes a NOR-based ring oscillator circuit to measure NBTI and a NAND-based ring oscillator circuit to measure PBTI. They also provide a third ring oscillator circuit that can measure either based on its inputs.

1. **Das, B.P.; Amrutur, B.; Jamadagni, H.S.; Arvind, N.V.; Visvanathan, V.; , "Within-Die Gate Delay Variability Measurement Using Reconfigurable Ring Oscillator," Semiconductor Manufacturing, IEEE Transactions on , vol.22, no.2, pp.256-267, May 2009**

Variations can be characterized as either die to die or within a single die. Within-die variations have both a spatially correlated component and a random component. Most of the existing techniques can adequately estimate the spatially correlated part, but random variation can affect logic gates independently. Random variations can originate from line edge roughness, oxide thickness variation and threshold voltage variation due to random dopant fluctuations. The random component needs to be measured at single gate level. This paper proposes a technique where individual gate delays can be measured. It describes a digitally reconfigurable ring oscillator structure that can be configured to use any logic gate. This provides gate delay information about individual gates in the circuit.

1. **Agarwal, Kanak, “On-die sensors for measuring process and environmental variation in integrated circuits.” IBM Corps. Austin, TX. 2010.**

Process variations are static in nature and do not change much with time. Environmental degradation has to be measured in real time because of its dynamic nature. Compact on-die monitoring circuits for measuring the variations have been presented in this paper. These structures can isolate process induced systematic and random variations in NFET and PFET devices. The circuit in the paper measures the frequency of a ring oscillator to determine the variation in the device. The novel part of the circuit, however, is that each of the inverters is tied to a virtual Vdd and Gnd through a PMOS or an NMOS. These devices can be individually turned on or off through a scan-in mechanism through a series of flip-flops. The user can only turn 1 device on at a time, scroll through the devices, and therefore measure the frequency variation due to the variation on the single device. This can be done with both the NMOS and the PMOS devices.

1. **Zhihao Jeff Lin, Costas Spanos, Linda Milor and Yung-Tao Lin, “Study of circuit sensitivity to interconnect variation.” IEEE. 1997.**

As device and interconnect dimensions are being scaled at an alarming rate, process uniformity and consistency are becoming key concerns for designers. It has been found that both layout and process parameters exhibit a significant amount of spatial variations. A sensitivity study of a circuit based on interconnect variations has been made here to relate the circuit performance and interconnect parameters. Monte Carlo simulations have been done to perform statistical analysis, reflecting closely to what happens in real world circuit fabrication. They found that inter-wire spacing is the most sensitive parameter and ILD thickness is the least sensitive.